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UNITED STATES PATENT APPLICATION

of

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and

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for

INTERLEVEL DIELECTRIC STRUCTURE

BACKGROUND OF THE INVENTION

This application is a divisional application of United States Patent Application Serial No. 677,514, filed on July 10, 1996, which is incorporated herein by reference.

1. The Field of the Invention

The present invention relates to the design and manufacture of interlevel dielectrics in the manufacture of semiconductor devices. More particularly, the present invention relates to the design and manufacture of interlevel dielectrics in the manufacture of semiconductor devices in which the dielectric constant of the interlevel dielectric is less than about 3.6.

2. The Relevant Technology

The continuing trend in the semiconductor industry of squeezing more and more circuit devices into a given area has resulted in significant improvements in the performance of individual integrated circuits and of electronic devices that employ integrated circuits. In a typical integrated circuit, individual circuit elements or groups of elements are generally electrically connected together by a metallization process, in which layers of metal are deposited and patterned to form metal lines which complete the circuit as designed. Multiple metal layers are often employed. Metal lines within patterned metal layers are insulated by layers known as interlevel dielectrics. The interlevel dielectrics insulate the metal lines from any undesired electrical contact both with other metal lines, whether in the same or another metal layer, and with other circuit elements.

The capacitance between two conductive materials is also affected by the material as well as the distance between them. The ratio of the capacitance between two conductors with a given material between them to the capacitance of the same two conductors with nothing (a vacuum) between them is known as the dielectric constant of the given material. Thus, a material with a high dielectric constant placed between two conductors increases the

The increasing density of integrated circuits has resulted in unneeded capacitance between metal lines in an integrated circuit due to metal line coupling capacitance. The unneeded capacitance slows circuit performance by causing too much buildup of charge where none is needed, thus slowing the buildup of charge at circuit elements where it is needed.

One way to decrease unneeded capacitance between metal lines in an integrated circuit is to decrease the dielectric constant of the material between them. Silicon dioxide, the material of choice for interlevel dielectrics, has a relatively high dielectric constant. Replacing silicon dioxide with a material having a lower dielectric constant would thus provide reduced capacitance. Useable materials having a low dielectric constant (e.g. less than about 3.6.) are generally much less stable than silicon dioxide and are thus unable to reliably protect the metal lines, and are unable withstand further processing.

One way to gain some of the benefits of low dielectric constant materials is shown in Figure 1. Figure 1 is a partial cross section of a partially formed integrated circuit device. A substrate or lower layer 12 has a first dielectric layer 14 comprised of a traditional dielectric material such as silicon dioxide. Lines of conductive material 16, typically metal, overlie first dielectric layer 14. A material with a dielectric constant lower than that of silicon dioxide 18 is located in between lines of conductive material 16. Lines of conductive material 16 together with low dielectric constant dielectric material 18 are covered by a second dielectric layer 21 comprised of a traditional dielectric material such as silicon dioxide. Second dielectric layer 21 together with first dielectric layer 14 isolate low dielectric constant dielectric material 18 from other portions of the integrate circuit. Second dielectric layer 21 allows further processing, including formation of contact holes for contacting lines of conductive material 16 such as contact hole 46 without exposing

While the structure shown in Figure 1 results in decreased capacitance between adjacent pairs of metal lines, further decrease is needed to allow increasing miniaturization and high speed operation of ever denser integrated circuits.

SUMMARY OF THE INVENTION

In accordance with the present invention, an interlevel dielectric structure includes first and second dielectric layers between which are located lines of a conductive material with a dielectric material in spaces between the lines of conductive material, with the lower surface of the dielectric material extending lower than the lower surface of lines of conductive material adjacent thereto, and the upper surface of the dielectric material extending higher than the upper surface of lines conductive material adjacent thereto, thus reducing fringe and total capacitance between the lines of conductive material. The dielectric material, which has a dielectric constant of less than about 3.6, does not extend directly above the upper surface of the lines of conductive material, allowing formation of subsequent contacts down to the lines of conductive material without exposing the dielectric material to further processing.

A preferred method for forming the interlevel dielectric structure includes providing an additional layer on a conductive layer on a first dielectric layer, then patterning both the additional layer and the conductive layer with an over etch into but not through the first dielectric layer, to form conductive lines with spaces therebetween. A dielectric material is then deposited to fill the spaces and is then etched or chemically mechanically polished back to the additional layer on the conductive layer. The additional layer on the conductive layer is then optionally removed before a second dielectric layer is deposited over all.

Another preferred method for forming the interlevel dielectric structure includes providing a conductive layer on a first dielectric layer, then patterning the conductive layer with an over etch into but not through the first dielectric layer to form conductive lines with spaces therebetween. An additional layer is then deposited by a method providing poor step [illegible] The additional layer is then optionally etched and a dielectric material is then

polished back to the additional layer. The additional layer is then optionally removed before a second dielectric layer is deposited over all.

Yet another preferred method for forming the interlevel dielectric structure includes providing a metal layer on a first dielectric layer, then patterning the metal layer with an over etch into but not through the first dielectric layer to form metal lines with spaces therebetween. A thin layer of silicon dioxide is then deposited by a method providing preferential deposition on the upper surfaces of the metal lines. The thin layer of silicon dioxide is then optionally etched, and a dielectric material is then deposited to fill the spaces and is then etched or chemically mechanically polished back. A second dielectric layer is then deposited over all.

The above briefly described methods allow reliable formation of a desired interlevel dielectric structure, which structure provides reduced total capacitance between adjacent conductive lines needed for further miniaturization of integrated circuits.

BRIEF DESCRIPTION OF THE DRAWINGS

In order that the manner in which the above-recited and other advantages and objects of the invention are obtained may be more fully explained, a more particular description of the invention briefly described above will be rendered by reference to specific embodiments and applications thereof which are illustrated in the appended drawings. Understanding that these drawings depict only typical embodiments and applications of the invention and are not therefore to be considered to be limiting of its scope, the invention will be described and explained with additional specificity and detail through the use of the accompanying drawings in which:

Figure 1 is a partial cross section of a partially formed integrated circuit device.

Figure 2 is a partial cross section of a partially formed integrated circuit device having a structure formed during the practice of a method of the present invention.

Figure 3 is a partial cross section of a partially formed integrated circuit device for use with a method of the present invention.

Figure 4 is a cross section of the structure shown in Figure 3 after further processing, and having a structure formed by a method of the present invention.

Figure 5 is a partial cross section of a partially formed integrated circuit device showing features formed during the practice of a method of the present invention.

Figure 6 is a partial cross section of a partially formed integrated circuit device depicting facet etching of a bread-loafed dielectric on metallization lines.

Figure 7 is a cross section of the structure shown in Figure 5 after further processing, and having a structure formed by a method of the present invention.

Figure 8 is a partial cross section of a partially formed integrated circuit device

Figure 9 is a cross section of the structure shown in Figure 8 after further processing, having a structure formed by a method of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention introduces an interlevel dielectric structure having a dielectric material between conductive lines with a lower surface of the dielectric material below a lower surface of the conductive lines, and an upper surface of the dielectric material above an upper surface of the conductive lines. The present invention also provides various methods for constructing the inventive structure. Because silica glass is used extensively in this art as a dielectric, and its dielectric constant is about 3.8, we define the interlevel dielectric material as one having a dielectric constant below about 3.6, preferably below about 2.9, and most preferably below about 2.2.

A preferred embodiment of the structure of the present invention is shown in Figure 2. A substrate or underlying layer(s) 12 of a semiconductor device is overlaid with a first dielectric layer 14, typically comprised of silicon dioxide, and having an upper surface 22. Lines of conductive material 16 with spaces therebetween extend (perpendicular to the plane of Figure 2) along upper surface 22 of first dielectric layer 14. Each of the lines of conductive material 16 has a lower surface 24 and an upper surface 26, with lower surfaces 24 being in contact with upper surface 22 of first dielectric layer 14. Lines of conductive material 16 are typically metal such as aluminum or copper, but may be comprised of other conductive materials such as polysilicon, aluminum, copper, tungsten, and multiple layers of TiN Al TiN, TiN Al Ti, W TiN Ti, or any combinations thereof.

A second dielectric layer 20 overlies lines of conductive material 16, with a lower surface 28 of second layer of dielectric material 20 being in contact with upper surfaces 26 of lines of conductive material 16.

Dielectric material 17, comprised of polytetrafluoroethylene (PTFE) or other suitable [illegible] between lines of conductive material 16. Dielectric

material 16 adjacent thereto, and a lower surface 30 lower than the lower surfaces 24 of lines of conductive material 16 adjacent thereto.

The extension of dielectric material 17 below and above lines of conductive material 16 significantly reduces capacitance between adjacent pairs of lines of conductive material 16.

The electric field formed by a potential difference applied across an adjacent pair of lines of conductive material 16 is strongest in a direct line and centrally between the adjacent pair, such as along dashed line N in Figure 2. But the electric field so formed also extends to a fringe area not in a direct line between the adjacent pair, such as along dashed line F in Figure 2. The field in this area, called the fringe, is associated with a portion of the total capacitance, the portion called herein "fringe capacitance," between the adjacent pair.

The portion of the total capacitance included in fringe capacitance increases as aspect ratio (height/width) of lines of conductive material 16 decreases, and can be a significant fraction of total capacitance at low aspect ratios. The extension of dielectric material 17 below and above lines of conductive material 16 provides a low dielectric material in the fringe areas of the electric field, thus reducing fringe capacitance and total capacitance accordingly.

While dielectric material 17 extends below and above lines of conductive material 16, it does not extend directly over surface 26 or under surface 24. This allows formation of contact holes such as contact hole 48 without exposing dielectric material 17 to processing agents that could degrade dielectric material 17 or upper surface 26 at contact hole 48.

The above structure and variations thereon may be formed in a variety of ways, presently preferred examples of which will be described below.

One method of forming a structure of the present invention includes

then forming a conductive layer 34 and an additional layer 36 thereover, as shown in Figure 3. Conductive layer 34 and additional layer 36 are then patterned by forming and patterning a mask layer over additional layer 36, and then etching additional layer 36, conductive layer 34, and a portion of first dielectric layer 14 at areas that are left exposed through the mask layer. This results in spaces between adjacent remaining portions of conductive layer 34.

Dielectric material 17 is then deposited to fill these spaces, and then removed from the top downward to at least the top of the remaining portions of additional layer 36 by an etch back or by chemical mechanical polishing. A second dielectric layer 21 is then deposited over the substrate, resulting in the structure shown in Figure 4.

In Figure 4, lines of conductive material 16 are formed of the remaining portions of conductive layer 34. Dielectric material 17 is deposited between lines of conductive material 16. If additional layer 36 is comprised of a suitable dielectric such as silicon dioxide, the remaining portions of additional layer 36 may be incorporated into the inventive structure as shown. Thus the remaining portion of additional layer 36 in Figure 4, together with second dielectric layer 21, correspond to the depiction seen in Figure 2 as second dielectric layer 20.

If additional layer 36 is not a dielectric, such as if titanium is used, for example, then the remaining portions of layer 36 shown in Figure 4 are removed by an appropriate process immediately before the deposition of second dielectric layer 20. This alternative additional process step results in a structure like that which is shown in Figure 2.

Another preferred method of forming a structure of the present invention includes providing a first dielectric layer over a substrate or an underlying layer, then depositing and patterning a conductive layer over the first dielectric layer. During patterning of the

etched partially with the same pattern. Next, an additional layer is deposited over the patterned metal layer by a deposition method having poor step coverage.

The results of the above steps are shown in Figure 5. First dielectric layer 14 has been formed on substrate or underlying layer 12, and a conductive layer has been deposited and patterned, leaving lines of conductive material 16. Additional layer 38 has been deposited by a deposition method having poor step coverage. This results in additional layer 38 being formed substantially only on the upper surfaces of lines of conductive material 16 as shown.

If additional layer 38 is comprised of a suitable dielectric material, the further process steps may proceed as before, with deposition and partial top-down removal of dielectric material 17 and deposition of second dielectric layer 21, resulting in the structure shown in Figure 7. The remaining portions of additional layer 38 are incorporated into the inventive structure as shown, so that the remaining portion of additional layer 38 in Figure 5 together with second dielectric layer 21 in Figure 7, correspond to the depiction seen in Figure 2 as second dielectric layer 20.

Silicon dioxide is the currently preferred material for additional layer 38, with deposition by a silane and oxygen plasma enhanced chemical vapor deposition (PECVD) being the preferred poor step coverage deposition method.

Figure 6 illustrates an optional etch step that may be included immediately after deposition of additional layer 38 to remove lateral buildup of additional layer 38. The preferred etch is a facet etch, and is preferably performed in an argon or an argon-plus-fluorine based plasma. In a facet etch, additional layer 38 is etched slower at a top surface thereof than it is etched at a corner thereof which connects the top surface to a lateral surface thereof. The facet etch has the effect of removing substantially all of the lateral buildup

at the base of the lines of conductive material 16 and first dielectric layer 14 interface. A continuous but thin lateral layer of additional layer 38 also deposits down the sides of lines of conductive material 16. Further processing as above then results in a structure like that which is shown in Figure 4, with the remaining portions of layer of additional material 36 corresponding to the remaining portions of additional layer 38. The redeposited fraction of additional material 38, however, remains thinly on the sides of lines of conductive material 16 and first dielectric layer 14.

If additional layer 38 is not a dielectric, or is otherwise not suitable to remain in place in the inventive structure, then additional layer 38 is removed by an appropriate process immediately before the deposition of second dielectric layer 21. This alternative additional process step results in a structure that is like that shown in Figure 2.

In yet another presently preferred method for forming a structure of the present invention, a first dielectric layer is provided over a substrate or an underlying layer, then a metal layer is deposited and patterned to form metal lines over the first dielectric layer. During patterning of the metal layer, the metal layer is over etched such that the first dielectric layer is etched partially with the same pattern. A thin silicon dioxide layer is then deposited conformably over the metal lines by a deposition process that deposits preferentially on the upper surface of the metal lines.

The above process results generally in the structure shown in Figure 8. First dielectric layer 14 is formed on substrate 12. Metal lines in the preferred form of aluminum lines 40 have been formed on first dielectric layer 14, and first dielectric layer 14 has been over etched in the same pattern as aluminum lines 40. A titanium nitride film 42 from a photolithography process used to pattern aluminum lines 40 remains on the upper surface of aluminum lines 40. While not required, inclusion of titanium nitride film 42 is presently

The preferred deposition process for selectively depositing a thin silicon dioxide layer 44 is an ozone based TEOS process, which preferentially deposits on TiN over silicon dioxide. Preferably, silicon dioxide layer 44 will be deposited only on titanium nitride film 42 and not on the sidewall of aluminum lines 40 as shown in Figure 8.

After deposition of silicon dioxide layer 44, the process may continue as with the other above processes by deposition and partial removal of a dielectric material 17, followed by deposition of second dielectric layer 21, resulting in the structure shown in Figure 9. Silicon dioxide layer 44 is incorporated into the inventive structure as shown, so that silicon dioxide layer 44 together with second dielectric layer 21 correspond to the depiction seen in Figure 2 as second dielectric layer 20.

As an alternative process step, an etch such as a facet etch in an argon or an argon-plus-fluorine based plasma may be performed on silicon dioxide layer 44 after the deposition thereof.

The present invention may be embodied in other specific forms without departing from its spirit or essential characteristics. The described embodiments are to be considered in all respects only as illustrated and not restrictive. The scope of the invention is, therefore, indicated by the appended claims and their combination in whole or in part rather than by the foregoing description. All changes which come within the meaning and range of equivalency of the claims are to be embraced within their scope.

What is claimed and desired to be secured by United States Letters Patent is